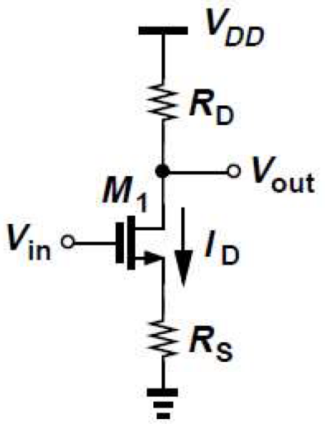
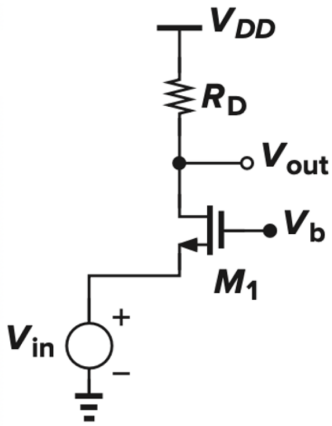
NX-422 Exercise 4, Implantable Electronics

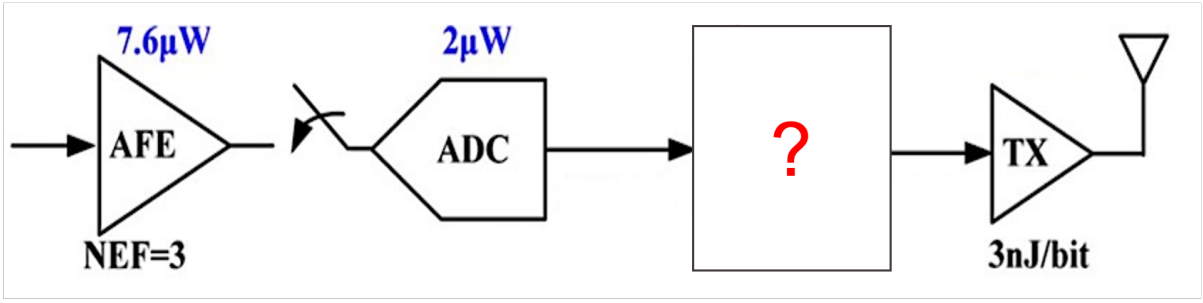
1. For the CMOS amplifier shown below, draw the small-signal model and find the voltage gain.



2. Draw the small-signal model of a common-gate amplifier shown below and find the voltage gain.



3. Consider a neural interface with the following signal chain. The power consumption of the amplifier (AFE) is 7.6 µW for single-channel spike or action potential (AP) recording. The ADC has 10 bits of resolution and consumes 2 µW of power. The frequency range for AP is (0.3-10 kHz).



How much data reduction after the ADC is required to satisfy a total power budget of <120 µW for the system, assuming the ADC samples inputs at the Nyquist rate and data compression (DSP) consumes negligible power?

4. For the following capacitive-feedback neural amplifier, derive the equation for the transfer function Vout(s)/Vin(s). Assume the OTA has a large gain. What is the mid-band gain of the amplifier?